ARMAG Ongoing Research Summary

The primary goal of ARMAG [Advanced RF and Mixed-Signal Applications Group] is development of innovative circuits and system level solutions for RF and mixed-signal applications. Research objective of ARMAG are inline with industry demands and is ensured by regular interaction with the industry members. As part of the NSF Center for Design of Analog and Digital Integrated Circuits (CDADIC), an industry and university consortium, ARMAG strives to create breakthroughs beneficial to the industry.

The following document highlights some of the recent research work being carried out at ARMAG.

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1. Low Power Low Noise Sub-Harmonic Injection Locked V-Band Beamforming Receiver

Introduction:

The unlicensed 8-10 GHz bandwidth available in V-band all over the world has led to the possibility of designing commercial multi-gigabits per sec wireless communication applications. Such high data rate communication can open the door for new applications like instant wireless sync between devices, wireless display, cordless computing and wireless LAN. However, any commercial application of mm-wave or higher frequency needs to achieve sub-watt power consumption in order to be integrated in mobile devices. Since most of the current state of the art mm-wave beamforming architectures consume watt level power, basic architectural changes are required to lower power consumption. In this proposal, a novel low noise LO phase shifting architecture with lower power consumption is proposed. The proposed V-band architecture and sub-block design techniques can be used in mm-wave (Ka and higher band) beamforming receiver applications.

Abstract:

There has been a surge of activities in V-band beamforming for commercial applications. Most current beamformers are designed based on a modular approach using either digital phase shifting, RF phase shifting or LO phase shifting. This modular approach to reduce noise in LNA and increase linearity leads to high power consumption. In this project, we propose a system optimization by integrating the RF-IF convention and LO power optimization by using a sub-harmonic injection locked self-oscillating mixer for mm-wave beamforming applications. The objective of this proposal is to investigate the design of low power low noise highly linear V-band beamforming receiver architecture with an emphasis on system level optimizations. Since loss of passive RF phase shifting is avoided, RF frontend can be designed to operate around process Fmin by use of noise cancelling LNA architecture. In addition, significant power savings without performance degradation can be achieved using novel sub-harmonic injection locking VCO with bulk-driven current reused mixer and low frequency LO distribution network.

The proposed project will present novel beamforming architecture that can achieve low power and low noise. Such architecture is crucial for next generation commercial and radar communication and will open up windows to new applications and reduction in cost of Si-based mm-wave beamformers.

2. Highly Linear MMICs for Wideband (12-40 GHz) Transceiver Beamformer Applications

Introduction:

Beamformer chipsets based on silicon technologies have been developed in industry and academia. Though most of them have been developed for narrow band applications, a single

beamformer spanning multiple bands is becoming more attractive as a cost effective solution. In addition, performance requirements such as higher linearity, low noise figure and gain controllability for each single channel are becoming more stringent. With this study, we propose an ultra-wideband single RF channel beamforming transceiver with low power, high linearity and gain controllability for multi-band beamformer applications.

Abstract:
The existing beamforming systems on silicon are mostly narrow band and span only a few bands of interest. Conventional techniques that are applied to improve bandwidth and linearity are not sufficient to meet performance requirements for multi-band operations in the low voltage scaled silicon process. We propose to advance the current state-of-the-art TRx beamforming chip by optimizing the performance of each key sub-block in terms of linearity, bandwidth, and phase accuracy. A single channel transceiver beamformer will be developed which will be easily scalable to multi-channel TRx beamformers. The design of Ku to Ka band MMICs for beamformers is challenging in terms of the wide bandwidth, linearity, and power consumption. In addition, the high frequency devices suffer from model accuracy. Hence, the system architecture of the transceiver beamformer is carefully defined taking into consideration linearity, bandwidth, gain, noise, phase accuracy, power consumption, process invariance and scalability to multi-beam applications. Based on silicon technologies, key sub-blocks including low noise amplifier, wideband phase shifter, highly linear VGA with reduced phase variation and low complexity power amplifier has been investigated and implemented. A novel method to enhance bandwidth of quadrature phase shifter is proposed. Novel design methodologies are utilized to enhance bandwidth and linearity and reduce power consumption of LNA, VGA and PA.

A wideband beamformer transceiver with high linearity and low power has been developed. The transceiver consists of sub-blocks including LNA, phase shifter, VGA and PA. A single channel 12-40 GHz beamforming receiver has also been implemented. Multi-band operation will help in the use of the single wideband beamformer for multiple applications.

3. Development of 8-channel Ku, L/S/C/X, K/Ka, W band receive/transmit beamformers

Introduction:

In traditional omnidirectional communication systems, a large portion of the electromagnetic energy is wasted because the transmitters radiate in all directions and only the transmitted power in a certain direction will reach the intended receivers. The beamformers, on the other hand, radiate and receive signals in a certain direction with high power efficiency. Besides, directional signal transmission has advantages in terms of interference rejection and signal-to-noise ratio improvement. Hence at frequencies where path loss is significant, beamforming is utilized.

Abstract:
In our research, we developed or are developing low power, highly linear 8-channel receive/transmit beamformers in a SiGe technology for several frequency bands, such as Ku band (10-13 GHz for Rx and 12.5-14.7 GHz for Tx), L/S/C/X band (0.8-12 GHz), K/Ka band (17-23 GHz for Rx and 27-31 GHz for Tx) and W band (94 GHz). In multi-channel beamformer designs, gain/phase imbalance between channels is one of the most critical performance criteria. To minimize the imbalance, symmetrical layout is carefully designed for power supplies to maintain similar IR drops from the power pad to the supplies of each channel. Phase stability determines the accuracy of the beam, which is also an important factor in beamformer designs. To reduce the phase variations introduced by changes of channel gain, compensation bits for variable gain amplifier are proposed to maintain a constant output capacitance when the gain changes. ADS momentum is employed to model the inductors and capacitors as well as interconnections to accurately model the passives..

4. Low voltage wireless link for biomedical application

Introduction:
Biomedical sensors nowadays are mostly using wireline connections for data communications. This not only confines the free movement of the test subject, but also poses risk of infection if the sensors are implanted. To solve these problems, wireless sensor is the best choice.

Abstract:
The objective of this research is to design low-cost low-power wireless transceivers that are uniquely desirable in applications like industrial monitoring, home automation, and biomedical sensors. Long battery life and small form-factor are extremely crucial in those applications, especially for implantable sensors. Therefore, low-power designs in architecture level, such as direct-conversion, injection-lock receivers, as well as in circuit levels, e.g., body-enabled design, switchless RF front-end, and current-reuse techniques are being investigated. Moreover, for biomedical applications such as neural-recording, the raw data rate could be as high as several hundreds of Mbps. Accordingly, novel wideband transceiver design techniques will be developed.

We have designed a 2.4-GHz wireless transmitter for biomedical applications that has an energy efficiency of 22-pJ/bit and can transmit at >100Mbps data rate. In addition, a 0.75 – 1 GHz low-IF multiband wireless transceiver for Zigbee applications has also been developed.

5. Millimeter-Wave Transceiver for Wireless Network-on-Chip

Introduction:

Recently demonstrated multi-core processors comprise up to 100 cores. Global interconnects within these high-performance Systems-on-Chips (SoCs) become a critical bottleneck in terms of both latency and power consumption. As one of the promising solutions, the Network-on-Chip (NoC) is able to outperform the mainstream bus architectures that consist of long interconnects. However, latency remains an impediment due to the inherent multi-hop communication mechanism of the wired NoC. Other emerging alternatives that could provide one-hop links still have their own limitations: 3D ICs with inductive or capacitive coupling require very close proximity with precise alignment, which also creates issues with heat dissipation. Optical interconnect, although having the advantage of high data rate and low latency, is incompatible with the commonly used CMOS technology.

Abstract:

The objective of this research is to design millimeter-wave wireless transceivers that can handle the data rate of tens of Gb/s, while maintaining an energy efficiency of around 1 pJ/bit. Such a highly efficient wireless transceiver is an essential building block in the wireless network-on-chip (WiNoC) architecture. In future multi-core VLSIs that contain hundreds of cores, the conventional network-on-chip (NoC) architecture will not only consume a significant amount of power, but also entail multiple hops for data to transmit from one core to another. WiNoC is a competitive alternative which can provide direct one-hop links for distant cores. Moreover, to cope with the demand of “green” computing, we’re seeking innovative methodologies to reduce the power consumption of the mm-wave transceivers.

We have designed several circuit building blocks for the millimeter-wave transceiver, such as a wideband LNA that has a bandwidth of 18 GHz, a low-power bulk-driven down-conversion mixer, a high-speed OOK modulator and TX front-end, as well as a 60-GHz injection-lock VCO.

6. Power management system for energy harvesting

Introduction:

To maximize the power output from individually operated SMFCs, their anode and cathode electrodes have to be electrically disconnected. A power management system has to harvest energy from each individual SMFC and store the accumulated energy in one storage device. Another challenge is to build a low-voltage and self-sustained power management system that can efficiently harvest the limited energy source. It has been shown that it is possible to generate watt level high power intermittently using sediment microbial fuel cells (SMFCs). Scale up issues of SMFCs limits continuous production of watt level power. To produce more power, larger electrodes are needed. However, a larger SMFC does not increase output current linearly as originally expected. Furthermore, deploying extremely large electrodes is difficult, and the

system is prone to failure. To solve this inherent energy scaling issue of SMFCs, an innovative approach is proposed.

Abstract:

The goal is to develop a new power management system (PMS) to produce continuous high power by harvesting energy from many individually operated SMFCs. The proposed scale-up energy harvesting PMS's main components are a low voltage charge pump, a low voltage DC/DC converter, harvest and control unit, and energy storage devices (capacitors). The charge pump will initially start up and/or repower the system when necessary. The energy storage devices will ensure that enough charge is available to power the circuit. The DC/DC converter will supply the necessary voltage to run the control unit. Finally, an innovative harvest and control system built from discrete components will efficiently accumulate energy from individually operated SMFCs and store it into a storage capacitor.

7. Wireless sensor nodes for food quality monitoring

Introduction:

Quality control and monitoring of perishable goods during transportation and delivery services is a critical concern for producers, suppliers, transport decision makers and consumers. The major challenge is to ensure a continuous quality control chain from producers to consumers in order to guarantee prime condition of goods. The monitored and controlled environmental parameters are temperature, humidity, and shock. These parameters are sensed by sensor motes, which can relay and transmit sensed data to a base station, where the information can be processed and analyzed. Zigbee has been widely used as a communication protocol for sensed data transmission. To lower the operating cost and increase the effectiveness of sensor motes, low power consumption, robustness and flexibility of use are required. A new sensor mote is proposed with an innovative energy-aware operating algorithm, and RFID technology is integrated to expand the usability of sensor motes.

Abstract:

The new sensor mote is designed based on TelosB platform running tinyOS. The new energy-aware operating algorithm includes wake-on sensing and wake-on radio communication. With wake-on sensing, the control unit of a mote is only activated when there are changing events in the environment, such as temperature change. The same principle applies to wake-on radio communication, in which the control unit is woken up when there is necessary communication among sensor motes. These wake-on modes allow the control unit to remain idle most of the time, which lowers power consumption. RFID transponders will be integrated to the motes, which will allow retrieval of sensed data by RFID readers. This allows application of the sensor motes in places where Zigbee network is not available.

8. Enveloped tracking high efficiency and linear CMOS power amplifier

Introduction:

Recently, as high speed wireless data communication has become popular, 4th generation wireless communication systems such as WiMax and Long Term Evolution (LTE) are being rapidly deployed. To provide higher data rates, these systems require modulated signals with high peak-to-average power ratio (PAPR) and broad instant frequency band. As the PAPR of the signal increases, the efficiency of the system at an average power level gets worse. Among all the components of the system, the power amplifier in the transmitter has the most critical influence on overall system power efficiency. Besides the requirement for high efficiency, another important requirement for the RF transmitter is low cost. So far, most power amplifier integrated circuits (ICs) are based on GaAs processes which are more expensive than silicon CMOS processes. In general, CMOS power amplifiers perform worse than their GaAs counterparts. To achieve high efficiency, high performance, and low cost, a fully integrated CMOS envelope tracking power amplifier integrated circuit will be designed.

Abstract:

A CMOS power amplifier IC will be designed for long-term evolution (LTE) applications. In order to comply with the LTE specifications for linearity, the power amplifier will also include a simple linearization method. The load network, incorporating matching and parallel combining circuits, will be designed to have low loss and small chip area based on 3-D EM simulation. The bias modulator, which has input of the base-band envelope signal and supplies the envelope signal to the power amplifier as its drain bias, should be designed to have high speed operation of least about 20MHz, and high efficiency over the wide signal dynamic range of the envelope signal. Finally, both the CMOS power amplifier and bias modulator will be integrated in a single chip.

9. Dynamic voltage frequency scaling for integrated system

Introduction:

Dynamic voltage frequency scaling (DVFS) offers great potential to reduce the power dissipation in a large system-on-chip (SOC) with multiple cores and processors. It can achieve power reduction by adjusting both frequency and supply voltage of the system adaptively to changing workloads. To exploit the full potential of DVFS, high speed and high efficiency regulators are needed to adjust voltage within the order of nanoseconds. Furthermore, these regulators are preferred to be fully integrated on chip, which helps lower cost and provide the flexibility to implement multiple power domains in an SOC. Our research is to develop and design a high speed and high efficiency fully integrated switching regulator targeting DVFS application.

Abstract:
Switching regulators are commonly used for their higher energy-conversion efficiency than their linear counterparts. To meet the speed requirement of DVFS application, the switching frequency has to be increased beyond 100 MHz. Unfortunately, switching loss increases proportionally to switching frequency. To reduce this loss, techniques such as zero-voltage-switching and adaptive switch size can be used. At such high frequency, the sizes of passive components such as inductors and capacitors are small enough to be implemented on chip. However, on-chip metal track inductors typically have low quality factor, which degrades efficiency. On package inductors, bond wire inductors, and extra thick metal layer are some popular solutions to provide high quality integrated inductors.